CLAIMS

What is claimed is:

1. A lighting system for graphics processing, comprising:

(a) a plurality of input buffers adapted for being coupled to a transform system for receiving vertex data therefrom, the input buffers including a first input buffer, a second input buffer, and a third input buffer, wherein an input of the first buffer, the second input buffer, and the third input buffer is adapted for being coupled to an output of the transform system;

(b) a multiplication logic unit having a first input coupled to an output of the first input buffer and a second input coupled to an output of the second input buffer;

(c) an arithmetic logic unit having a first input coupled to an output of the second input buffer and a second input coupled to an output of the multiplication logic unit, wherein an output of the arithmetic logic unit is coupled to the output of the lighting system;

(d) a register unit coupled to an output of the arithmetic logic unit;

(e) a lighting logic unit having a first input coupled to the output of the arithmetic logic unit, a second input coupled to the output of the first input buffer, and an output coupled to the first input of the multiplication logic unit; and

(f) memory coupled to at least one of the inputs of the multiplication logic unit and the output of the arithmetic logic unit, the memory having stored therein a plurality of constants and variables for being used when processing the vertex data.

2. The system as recited in claim 1, wherein the output of the third buffer is coupled to the output of the lighting system via a delay.

3. The system as recited in claim 2, wherein the output of the arithmetic logic unit and the output of the third input buffer are coupled to the output of the lighting system by way of a multiplexer.

4. The system as recited in claim 1, wherein the output of the multiplication logic unit has a feedback loop coupled to the second input thereof.

5. The system as recited in claim 1, wherein the second input of the lighting logic unit is coupled to the output of the first input buffer via a delay.

6. The system as recited in claim 1, wherein the output of the lighting logic unit is coupled to the first input of the multiplication logic unit via a threaded first-in first-out register unit.

7. The system as recited in claim 1, wherein the output of the lighting logic unit is coupled to the first input of the multiplication logic unit via a conversion module adapted for converting scalar vertex data to vector vertex data.

8. The system as recited in claim 1, wherein the memory has a read terminal coupled to the first and second input of the multiplication logic unit.

9. The system as recited in claim 1, wherein at least one of the inputs of the arithmetic logic unit and the multiplication logic unit include multiplexers.

10. The system as recited in claim 1, wherein the memory has a write terminal coupled to the output of the arithmetic logic unit.

11. The system as recited in claim 1, wherein the multiplication logic unit includes three multipliers coupled in parallel.

12. The system as recited in claim 1, wherein the arithmetic logic unit includes three adders coupled in series and parallel.

13. The system as recited in claim 1, wherein register unit includes two sets of registers each having an output coupled to a first input of an associated multiplexer which has a second input coupled to the input of the corresponding set of threaded registers.

14. A lighting system for graphics processing, comprising:

(a) at least one input buffer adapted for being coupled to a transform system for receiving vertex data therefrom, wherein an input of the input buffer is adapted for being coupled to an output of the transform system;

(b) a multiplication logic unit having a first input and a second input coupled to an output of the input buffer;

(c) an arithmetic logic unit having a first input coupled to an output of the input buffer and a second input coupled to an output of the multiplication logic unit, wherein an output of the arithmetic logic unit is coupled to the output of the lighting system;

(d) a first register unit having an input coupled to the output of the arithmetic logic unit and an output coupled to the first input of the arithmetic logic unit;

(e) a second register unit having an input coupled to the output of the arithmetic logic unit and an output coupled to the first input and the second input of the multiplication logic unit;

(f) a lighting logic unit having a first input coupled to the output of the arithmetic logic unit, a second input coupled to the output of the input buffer, and an output coupled to the first input of the multiplication logic unit; and

(g) memory coupled to at least one of the inputs of the multiplication logic unit and the output of the arithmetic logic unit, the memory having stored therein a plurality of constants and variables for being used when processing the vertex data.

15. A method for providing a lighting system for graphics processing, comprising:

(a) connecting a plurality of input buffers to a transform system for receiving vertex data therefrom, the input buffers including a first input buffer, a second input buffer, and a third input buffer, wherein an input of the first buffer, the second input buffer, and the third input buffer is adapted for being coupled to an output of the transform system;

(b) coupling a first input of a multiplication logic unit to an output of the first input buffer and a second input of the multiplication logic unit to an output of the second input buffer;

(c) connecting a first input of an arithmetic logic unit to an output of the second input buffer and a second input of the arithmetic logic unit to an output of the multiplication logic unit, wherein an output of the arithmetic logic unit is coupled to the output of the lighting system;

(d) mating an input of a first register unit to the output of the arithmetic logic unit and an output of the first register unit to the first input of the arithmetic logic unit;

(e) pairing an input of a second register unit to the output of the arithmetic logic unit and an output of the second register unit to the first input and the second input of the multiplication logic unit;

(f) coupling a first input of a lighting logic unit to the output of the arithmetic logic unit, a second input of the lighting logic unit to the output of the first input buffer, and an output of the lighting logic unit to the first input of the multiplication logic unit; and

(g) connecting memory to at least one of the inputs of the multiplication logic unit and the output of the arithmetic logic unit, the memory having stored therein a plurality of constants and variables for being used when processing the vertex data.

16. A method for flagging in a graphics processing module, comprising:
(a) providing a graphics processing module adapted to be governed by a plurality of mode bits indicative of a status of a plurality of modes of process operations;
(b) processing the vertex data in the graphics processing module in accordance with the mode bits;
(c) outputting the processed vertex data; and
(d) setting at least one flag upon the vertex data satisfying predetermined criteria.

17. The method as recited in claim 16, wherein the graphics processing module is a lighting module.

18. The method as recited in claim 17, wherein a lighting logic unit of the lighting module sets the flag.

19. The method as recited in claim 16, and further comprising clamping a value of an attribute of the vertex data based on the setting of the flag.

20. A computer program embodied on a computer readable medium for flagging in a graphics processing module, comprising:
(a) a code segment for providing a graphics processing module adapted to be governed by a plurality of mode bits indicative of a status of a plurality of modes of process operations;
(b) a code segment for processing the vertex data in the graphics processing module in accordance with the mode bits;
(c) a code segment for outputting the processed vertex data; and
(d) a code segment for setting at least one flag upon the vertex data satisfying predetermined criteria.

21. The computer program as recited in claim 20, wherein the graphics processing module is a lighting module.

22. The computer program as recited in claim 21, wherein a lighting logic unit of the lighting module sets the flag.

23. The computer program as recited in claim 20, and further comprising a code segment for clamping a value of an attribute of the vertex data based on the setting of the flag.